Large-Scale Integration of Semiconductor Nanowires for High-Performance Flexible Electronics

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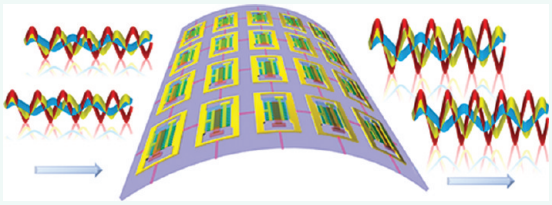
ABSTRACT



High-performance flexible electronics has attracted much attention in recent years due to potential applications in flexible displays, artificial skin, radio frequency identification, sensor tapes, *etc.* Various materials such as organic and inorganic semiconductor nanowires, carbon nanotubes, graphene, *etc.* have been explored as the active semiconductor components for flexible devices. Among them, inorganic semiconductor nanowires are considered as highly promising materials due to their relatively high carrier mobility, reliable control on geometry and electronic properties, and cost-effective synthesis processes. In this review, recent progress on the assembly of high-performance inorganic semiconductor nanowires and their applications for large-scale flexible electronics will be summarized. In particular, nanowire-based integrated circuitry and high-frequency electronics will be highlighted.

KEYWORDS: nanowire · monolayer · shear force · contact printing · assembly techniques · flexible electronics · high-frequency device · integrated circuitry

Flexible electronics refers to the technology that integrates electronic devices on flexible substrates. It can be implemented using flexible active materials such as amorphous silicon and organic semiconductors, conventionally.[1−12] However, due to the fundamental limits on material properties, mainly carrier mobility and material stability, these materials cannot offer promises for high-performance flexible electronics.[13−18] In contrast, synthetic inorganic semiconductor nanowires (NWs) are highly flexible due to submicrometer diameters,[19−23] and they have been fabricated into an assortment of electronic devices demonstrating carrier mobility up to 21 000 $cm^2/(V\cdot s)$,[19,20,24−29] and device oscillation frequency higher than 20 GHz.[30] In addition, the synthetic semiconductor NWs are typically grown with bottom-up chemical approaches with high-throughput and tailorable material properties such as shape, size, atomic composition, and doping concentration.[31−36] Thus they are extremely attractive for large-scale printable electronics with requirements on performance. It is worth noting that carbon-based nanomaterials including carbon nanotubes (CNTs) and graphene have also demonstrated spectacularly high mobility,[37−43] especially the latter has shown carrier mobility up to 20 000 $cm^2/(V\cdot s)$ at room temperature.[44] Nevertheless, CNTs face the challenge of controlling the conduction type and doping level precisely and reproducibly, while band gap opening in graphene is rather challenging.[39,45−48] On the other hand, semiconductor nanowires have demonstrated excellent mechanical flexibility.[19,20,25,49−54] and many different types of high mobility semiconductor NWs, such as core−shell Ge/Si NWs,[25,55] GaAs NWs,[56,57] InAs NWs,[58−60] *etc.*, have been successfully synthesized. These achievements have provided us with a vast choice of materials for nanowire-based high-performance flexible applications.

In this review article, we will summarize the state-of-art research progress on high-performance NW devices for large-scale flexible electronics. In general, these studies aim at developing a scalable platform for integration of NW devices on flexible substrate with fast operation speed, as schematically shown in Figure 1. It is evident that not only proper materials need to be identified but also a reliable and scalable NW assembly technique needs to be developed. As one of the major challenges toward

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NW-based large-scale electronics is lack of a scalable and printable approach for the assembly of NWs with reasonable alignment, density, and uniformity, we will begin with an introduction of technologies for large-scale semiconductor NW assembly, including flow-assisted alignment,[27,61] bubble-blown technique,[62] Langmuir–Blodgett approaches,[63–68] and contact/roll printing techniques.[25,51] With these approaches, large-scale NW-array-based thin film transistors have shown operation frequency up to 1.8 GHz.[69] Furthermore, all-NW integrated circuits have been successfully demonstrated.[19,50,70] These encouraging achievements have shown the promising potential and practical approaches to realize semiconductor NW-based large-scale high-performance electronics, which can enable a whole new generation of flexible electronics for computing, storage, communication, smart sensing, and beyond.

Nanowire Assembly on Flexible Substrates. Fabrication methods of synthetic NW materials have been well-documented, thus they are not the focus of this review. NW materials synthesized primarily by bottom-up growth methods have shown crystalline nature enabling fast carrier transport for high-performance electronic applications.[55,56,58,69,71–73] Briefly, individual NW devices are usually fabricated following such a process: NWs collected on a substrate are suspended in an organic solvent and then dispersed onto a device substrate. Thereafter, a photo- or electron-beam lithography process followed by metallization and lift-off is utilized to pattern metallic electrodes to the NWs.[33,35,73–75] Typically, such drop-casting of random aligned NWs results in a very low device yield. However, it is sufficient to study their fundamental properties of single NW concept-proof devices. Apparently, this method is not suitable for low-cost and mass production of NW devices on a large scale. The assembly of NWs with controlled orientations and interspacing over large areas is essential for the fabrication of complex logic circuits and high-performance devices in which randomness of NW alignment can lead to performance degradation such as deteriorated transistor gate electrostatic coupling.[70] In the past, significant effort has been invested on developing generic approaches to assemble NWs on various substrates, for instance, flow-assisted alignment,[27,61,76,78,88] Langmuir–Blodgett,[63–68] bubble-blown techniques,[62] electric-field-directed assembly,[79–82] and contact/roll printing techniques.[25,51,58,70,83–87] The advantages and disadvantages of these approaches are briefly summarized in Table 1 followed by the detailed discussions.

Flow-Assisted Nanowire Alignment. It is known that the motion of a fluid can create a shear force against a solid boundary.[61,88] This effect can be utilized to align NWs suspended in a solution. The orientations of NWs will be realigned to the flow direction of the fluid to minimize the fluid drag forces. Huang *et al.*[61] have further developed this technique to align NWs by confining the fluid in a microfluidic channel. In this flow-assisted assembly technique, schematically shown in Figure 2a, a flat substrate is covered by a poly(dimethylsiloxane) (PDMS) mold with a microchannel with width ranging from 50 to 500 μm and length from 6 to 20 mm. When flowing a suspension of NWs through the microchannel, the NWs can be assembled parallel to the flow direction. Figure 2b shows a scanning electron microscopy (SEM) image of NWs assembled on the substrate surface within microfuidic flow, showing that the NWs are aligned along the flow direction. This fluidic-directed assembly can extend over several hundreds of micrometers and is restricted only by the size of the microchannels. Huang *et al.* have also demonstrated high-performance p-Si NW transistors using this fluid-assisted alignment technique.[61] Periodic aligned NW arrays have also been demonstrated by Huang *et al.* by combining a surface modification technique with the flow-assisted assembly technique.[61] In this case, NH_2-terminated monolayers were patterned on the surface of a SiO_2/Si substrate in the shape of parallel stripes with a separation of a few micrometers. During the flow-assisted assembly process, the NWs are preferentially captured by the NH_2-terminated surface regions. The direction of the NWs is dominated by the shear force created by the fluidic flow in the microchannels. Therefore, both the controlled location and orientation of the NWs are achieved.

Furthermore, this flow-directed technology can be used to align the NWs into more complex and crossed NW structures, which are pivotal for constructing nanodevice arrays.[61,76,78,88] As shown in Figure 2c, crossed NW arrays can be obtained by a layer-by-layer deposition process, namely, by alternating the flow in

VOCABULARY: **monolayer** – a single, closely packed layer of insoluble nanowire (NW) film spread onto an aqueous subphase; **contact printing** – NWs assembly technology which enables the direct and controllable transfer of NWs from the growth substrate to the receiver substrate as highly aligned, parallel arrays with constant controllable pressure and direction; **flexible electronics** – electronic circuits which are assembled by mounting electronic devices on flexible plastic substrates, such as polyimide, PEEK, or transparent conductive polyester film; **high-frequency device** – electronic devices which are usually made of high mobility semiconductors. They can be operated at high frequencies in the GHz range or even in THz; **integrated circuitry** – an assembly of electronic components, such as transistors, diodes, resistors, and capacitors, *etc.*, as well as electronic interconnects, fabricated on a monolithic chip;

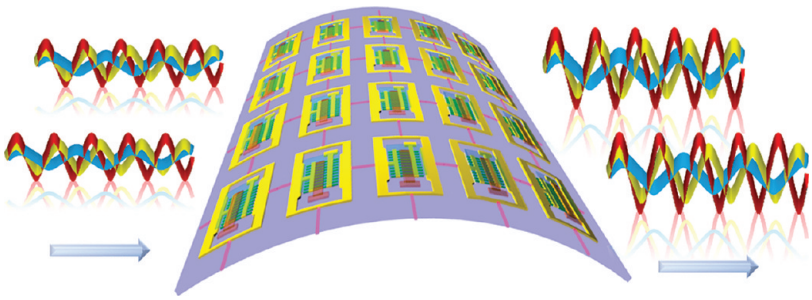

Figure 1. Schematic of printed NW array field-effect transistors integrated on a flexible substrate with high-frequency operation.

TABLE 1. Summary of NW Assembly Technologies

NW assembly technologies	advantages	disadvantages	examples	references
flow-assisted alignment in microchannels	(1) parallel and crossed NW arrays can be assembled (2) compatible with both rigid and flexible substrates	(1) area for NW assembly is limited by the size of fluidic microchannels (2) difficult to achieve very high density of NW arrays (3) NW suspension needs to be prepared first	Si, CdS, GaN, InP, GaP NWs	61, 76, 78, 88
bubble-blown technique	(1) area for NW assembly is large (2) compatible with both rigid and flexible substrates	(1) it is difficult to achieve high-density NW arrays (2) NW suspension needs to be prepared first	Si NWs	62
contact printing	(1) area for NW assembly is large (2) high-density NW arrays can be achieved (3) parallel and crossed NW arrays can be assembled (4) direct transfer NW from growth substrate to receiver substrate (5) compatible with both rigid and flexible substrates (6) NW assembly process is fast	(1) growth substrate needs to be planar (2) the process works the best for long NWs	Si, Ge, InAs, CdSe, Ge/Si core/shell, ZnO, SnO_2 NWs	25, 58, 70, 83–87, 101, 102, 105
differential roll printing	(1) area for NW assembly is large (2) high-density NW arrays can be achieved (3) direct transfer NW from growth substrate to receiver substrate (4) compatible with both rigid and flexible substrates (5) NW assembly process is fast	(1) growth substrate needs to be cylindrical (2) the process works the best for long NWs	Ge, ZnO NWs	51, 90
Langmuir– Blodgett technique	(1) area for NW assembly is large (2) High density NW arrays can be achieved (3) parallel and crossed NW arrays can be assembled (4) compatible with both rigid and flexible substrates	(1) NWs typically need to be functionalized with surfactant (2) the assembly process is slow and has to be carefully controlled (3) NW suspension needs to be prepared first	Si, Ge, ZnSe, VO_2 NWs	63–68
electric field-assisted orientation	(1) NWs can be placed at specific location (2) compatible with both rigid and flexible substrates (3) NW assembly process is fast	(1) patterned electrode arrays are needed (2) area for NW assembly is limited by the electrode patterning (3) NW density is limited (4) it works the best for conductive NWs (5) NW suspension needs to be prepared first	Au, Ag, Si, SiC, InP NWs	77, 79–82, 97

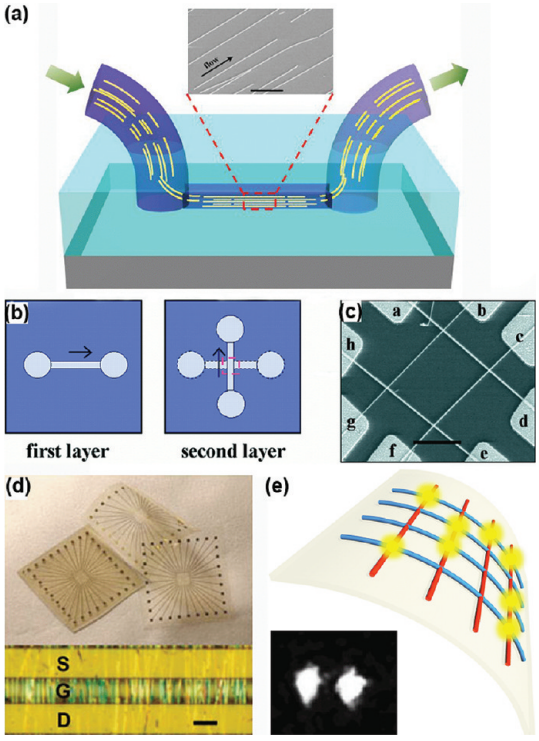

Figure 2. Fluidic flow-directed assembly of NWs. (a) Schematic of parallel NW arrays obtained by passing NW solution through a microchannel on a substrate. The inset is the paralleled NW SEM image. (b) Schematic and (c) SEM image of crossed NW matrix obtained by orthogonally changing the flow direction in a sequential flow alignment process. Reprinted with permission from ref 61. Copyright 2001 American Association for the Advancement of Science. (d) Upper photo is a picture of plastic devices with Si NW film. The plastic devices show high mechanical flexibility. Lower image is an optical micrograph of a locally gated NW-TFT. Reprinted with permission from ref 27. Copyright 2003 Nature Publishing Group. Scale bar, 5 mm. (e) Schematic of a flexible light-emitting display consisting of a crossed-NW LED array on a flexible plastic substrate. Inset: electroluminescence images of localized emission from forward-biased Si-GaN junctions. Reprinted from ref 100. Copyright 2003 American Chemical Society.

orthogonal directions through a two-step assembly process. The key feature of this layer-by-layer assembly strategy is that each layer is independent of the others. Therefore, various homo- and hetero-junctions can be fabricated at the crossed points. NWs with different conduction types (*e.g.*, p-Si and n-GaN NWs) in each step have been used to fabricate logic gates with computational functions and light-emitting diodes from the assembled crossbar NW structures (Figure 2c).[76,78] Interestingly, this NW assembly process is compatible with various types of substrates, including plastics. Figure 2e demonstrates assembled NW array thin film transistors (TFTs) and light-emitting diodes (LEDs) on a plastic substrate. Further measurements have shown that NW array TFTs have >100 $cm^2/(V \cdot s)$ field-effect mobility, which is significantly better than that of a-Si and organic semiconductors for flexible electronics.[22,27,69,70,89] Nevertheless, the main disadvantage of this technique is that the area for NW alignment is restricted by the size of the

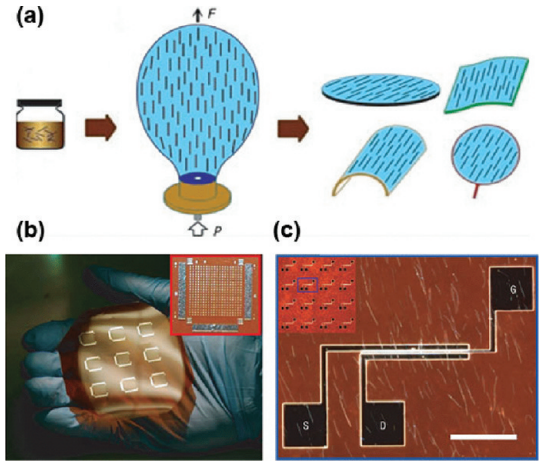

Figure 3. Bubble-blown assembly of NWs. (a) Schematic process flow of NW assembly. (b) Plastic substrate with Si NW device arrays. (c) Dark-field optical image of one top-gated Si NW FET device; the scale bar is 50 μm. Reprinted with permission from ref 62. Copyright 2007 Nature Publishing Group.

fluidic microchannels, and it is rather difficult to form a uniform shear force in a large channel.

Bubble-Blown Nanowire Assembly on a Plastic Substrate. The shear force created by the expansion of a bubble-blown film can also be utilized for large-scale assembly of NWs. Yu *et al.* developed a unique NW assembly technique based on this principle, and the process is schematically shown in Figure 3a.[62] Briefly, a homogeneous polymer suspension of NWs was first prepared then dispersed on a circular dye followed by blowing the dye into a bubble at controlled pressure and expansion rate.[62] During this process, the expansion caused shear force to align more than 85% of the NWs along the upward expansion with only $\pm 6°$ discrepancy.[62] Then the NWs can be transferred to rigid or flexible substrates by bringing them in contact with the bubble.[62] Figure 3b,c demonstrates Si NW arrays assembled on plastic substrate and resulting FET devices. In experiments, Si NWs were transferred to flexible plastic sheets up to 225×300 mm^2 and single-crystal wafers up to 200 mm in diameter. In principle, NW density within the film can be tuned by the concentration of the NW in the polymer suspension, thus large NW FET arrays could also be fabricated by this method. However, due to the expansion of the bubble, it is challenging to achieve close pack of NWs, thus NW density was modest ($\sim 0.04/\mu m^2$), which can also be seen from Figure 3c.[62] Therefore, it is not ideal for fabricating a high current output device with small dimensions.

Contact/Roll Printing Techniques. Recently, a novel and convenient contact printing technique for wafer-scale assembly of aligned and high-density NW arrays has been reported.[25,51,83] The contact printing method can align NWs into parallel arrays when transferred from the growth substrates to the receiver substrates

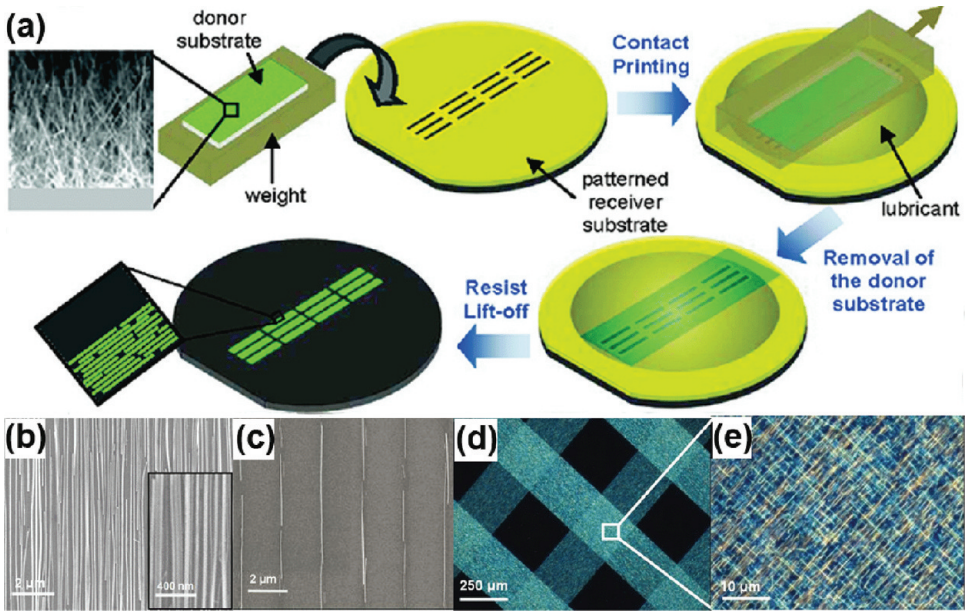

Figure 4. Contact printing of NWs. (a) Schematic of the process flow for contact printing of NW arrays. (b) SEM images of Ge NWs printed on a Si/SiO_2 substrate showing a highly dense and aligned monolayer of NWs. (c) SEM image showing regular array assembly of single Ge NWs at predefined locations on a Si/SiO_2 substrate. (d,e) Optical images of double layer printing for Si NW crossed assembly. Reprinted from ref 25. Copyright 2008 American Chemical Society.

directly and controllably for a wide range of electronic applications.[25,58,70,83−87,101,102,105] As shown in Figure 4a, this technique uses randomly grown NWs on a donor substrate sliding over a receiver substrate directionally. During this contact sliding process, NWs are realigned by the sliding shear force and are ultimately detached from the donor substrate when held by the van der Waals interactions with the contacted surface of the receiver substrate, bringing out the direct transfer of paralleled NWs to the receiver substrate (Figure 4b). In order to minimize the undesirable NW−NW friction and the uncontrolled breakage and discrete of NWs during the sliding process, a mixture of octane and mineral oil is used as a spacing layer between the two substrates.[25] Through reducing the interstitial mechanical friction, well-controlled transfer of the NW is achieved by chemical binding interactions between NWs and the surface of the receiver substrate.[25] Hence, the printed NW density is readily controlled by the suitable surface chemical modification.[25,83] Then the patterned resist is removed using a standard lift-off process after NW printing. With this technique, ~7 NW/μm high dense array of NWs (Figure 4b) and streams of single NWs (Figure 4c) have also been assembled.[25] In addition, NW crosses or controlled stacking of the NWs can be achieved by a two-step printing methodology.[25] Briefly, a layer of a paralleled NW array was first contact printed onto a receiver substrate. Then a thin film of poly(methyl methacrylate) was spin-coated onto the sample and served as a buffer layer, followed by a second printing step normal to the direction of the first layer. Finally, moderate O_2 plasma was used to etch away the polymer buffer. Thus the large arrays of NW crosses were formed, as shown in Figure 4d.

The contact printing technique is not only versatile but also, more importantly, highly scalable. The researchers successfully aligned parallel and dense NW arrays on a 4 in. Si wafer, shown in Figure 5a.[25] Note that the density of the NW films that are obtained by this contact printing process is comparable to those attained by the LB method and is much larger than those obtained by the bubble-blown technique. The high density of NWs is attractive for realizing dense arrays of single NW devices or high ON currents considering thin film transistors with parallel array NW channels. Figure 5b shows the SEM images of back-gated parallel arrayed NW FETs with different channel widths (single NW, 10 and 250 μm). Furthermore, printed parallel array Si NW diodes can also be fabricated on flexible plastic Kapton substrates, as shown in Figure 5c.

To further develop the NW contact printing approach, the researchers have grown NWs on cylindrical substrates then transferred NWs to various types of substrates with a roll printing method.[51] The principle of this unique roll printing technique is schematically shown in Figure 6a,b. Particularly, due to the larger diameter of the wheels on the two ends of the NW growth cylinder itself, as compared to that of the cylinder, the cylinder−substrate contact region slides laterally on the substrate while rotating around its own axis.[51] As discussed before, shear force applied to NWs caused by the sliding motion detaches NWs from the cylinder, meanwhile aligning them into parallel arrays, as shown in Figure 6b. It has been shown that this roll printing procedure is compatible with various types of substrates, including rigid Si, glass, and flexible paper

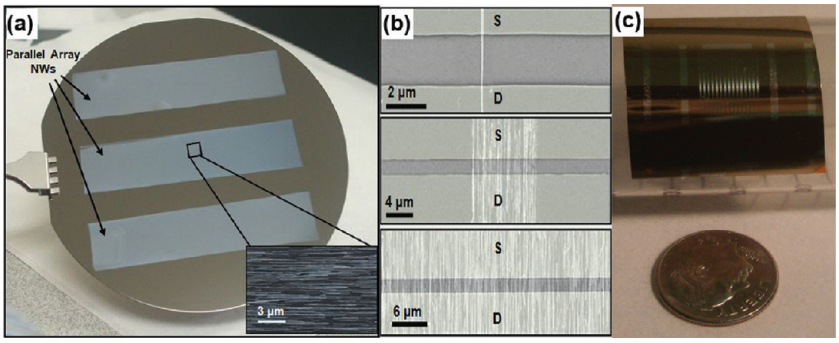

Figure 5. Wafer-scale NW printing and devices based on printed NW arrays. (a) Large area and highly uniform parallel arrays of aligned Ge NWs were assembled on a 4 in. Si/SiO_2 wafer by contact printing. (b) SEM images of parallel arrayed Ge/Si NW FETs with different channel widths (single NW, 10 and 250 μm). (c) Optical image of a diode structure fabricated on parallel arrays of p-Si NWs on a flexible plastic substrate. Asymmetric Pd–Al contacts are used to obtain Schottky diodes. Reprinted from ref 25. Copyright 2008 American Chemical Society.

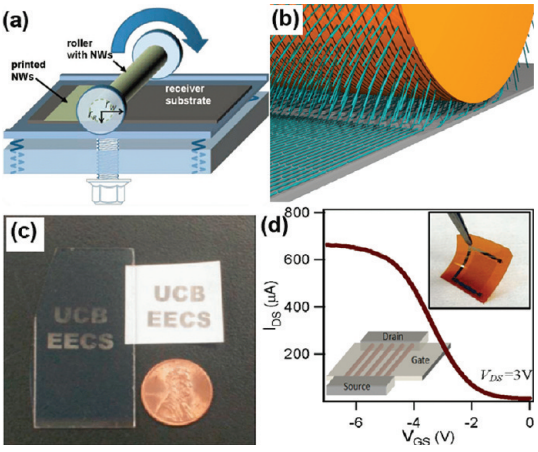

Figure 6. Differential roll printing. (a) Schematic of the differential roll printing setup. (b) Roll printing NWs onto the substrate. (c) Large area and aligned arrays of Ge NWs printed on glass and photography paper. The substrates were patterned using photolithography and functionalized with poly-L-lysine before printing to enable patterned assembly of NWs. (d) Parallel arrayed NW FETs on a plastic substrate. The bottom inset shows the schematic of the NW device structure, and the top inset is a photograph of the substrate after NW device fabrication. Reprinted with permission from ref 51. Copyright 2007 American Institute of Physics.

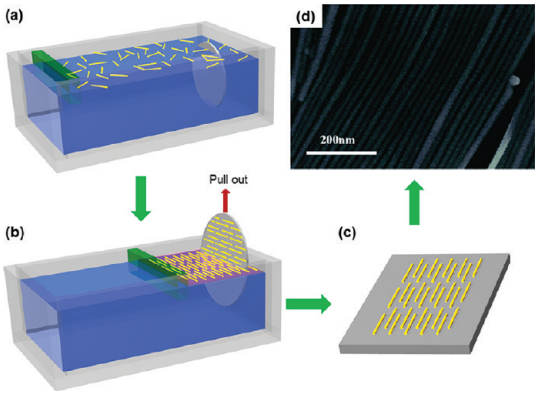

Figure 7. Langmuir–Blodgett assembly. (a) Random NWs suspended in the Langmuir–Blodgett trough. (b) Wafer being pulled vertically from the suspension in parallel with the lateral motion of the barrier. (c) Monolayer of parallel NW arrays assembled onto the substrate. (d) SEM image of paralleled Ge NW film transferred to the substrate by LB compression. Reprinted from ref 64. Copyright 2005 American Chemical Society.

and plastic (Figure 6c).[51] In addition, Figure 6d shows the roll-printed NW FETs on a flexible Kapton substrate using Ge/Si core/shell parallel array NWs as the channel material, with a NW density of ~6/μm, demonstrating high ON current. It is worth noting that this roll printing method is highly promising for roll-to-roll production of flexible devices by nature. Combining single-crystalline semiconductor NWs, high-performance flexible electronic devices can be fabricated with high-throughput using this technique.[91]

Other Approaches. Besides the aforementioned NW assembly methods, there are also several other techniques that have been developed to achieve NW assembly, such as Langmuir–Blodgett (LB) technique, electric field-assisted NW assembly,[77,79] and strain-release NW assembly.[92] These techniques will be briefly introduced below.

Langmuir–Blodgett (LB) technique is usually utilized to deposit one or more organic monolayers from the surface of a liquid onto a solid substrate by immersing the substrate into the liquid to form extremely thin films with a high degree of structure ordering.[63–65,67] It was found that this technique can also be used for the assembly of nanomaterials including nanoparticles, nanorods, NWs, nanotubes, and nanosheets.[65,93–96] To perform assembly of these materials with LB technique, they are typically functionalized by surfactants in order to form stable suspensions in the organic solvents.[63–68] The process of the LB technique can be briefly described as follows, which is shown in Figure 7. A NW–surfactant monolayer is first formed on a liquid surface in an LB trough. Then a barrier compresses the NW monolayer with an appropriate level of compression. The NWs with different orientations are realigned as parallel arrays with their

longitudinal axes perpendicular to the compression direction to reduce the surface energy of the liquid. The vertical-dipping or horizontal-lifting techniques are then used to deposit the monolayer of the aligned NWs onto a substrate. The distance between the parallel NWs can be controlled by the lifting speed and compression pressure.

Up-to-date, many researchers have used LB technique to assemble various NWs in large scales, for example, silver NWs,[63] Si NWs,[68] Ge NWs,[64] ZnSe NWs,[65] and VO_2 NWs.[67] In many works, the distance between the transferred NWs is adjusted from micrometer scale to well-ordered and close-packed structures by the compression process. The ability to assemble NWs with hierarchical structures makes the LB technique attractive for fabricating devices with complex structure. Hierarchical structures can be prepared by repeating the assembly process after altering the orientation of the substrate.[68] Although LB technique has demonstrated its versatility for NW assembly, the disadvantages of this technique rest in several aspects: NWs have to be surface functionalized; the LB process is slow, and the condition control is rigid, otherwise, NW array films are not uniform, as summarized in Table 1.

Polarization of materials in the electric field induces force parallel to the field which can be used to align semiconductor NWs.[77,79−82,97] Typically, such experiments are performed in a NW suspension where NWs are free to move and reorient. Electric field can be created by the pair electrodes on the supporting substrate. In this case, multiple NWs could be aligned parallel along the electrical field direction, and individual NWs could also be fixed at specific positions with controlled directionality. Furthermore, the alignment of NWs can be accomplished in a layer-by-layer fashion to fabricate crossed NW junctions through altering electrical field direction of consecutive NW solutions.[77]

Recent development of this technique combined dielectrophoretic force and fluidic NW alignment.[79] In this work, laminar flow of the NW suspension was established in a thin channel with a substrate patterned with pair electrodes serving as one side of the channel, as shown in Figure 8. In the stable flow, alternating electric field-induced dielectrophoretic force aligned NWs and trapped them between the pair electrodes. By balancing nanowire−nanowire interactions and dielectrophoretic, surface, and hydrodynamic forces, the researchers demonstrated self-limiting assembly of single NWs with 98.5% yield on 16 000 electrode sites covering 400 mm^2.[79]

Electric field alignment/assembly of NWs is a technique of importance, particularly for the case that NWs are required to be positioned at specific locations precisely. However, the major disadvantage of this technique rests in the need for prefabricated microelectrode arrays to generate electric field on chip; this can increase the complexity of the process and limit the scalability of the process.

Recently, a strain-release assembly method was developed to align inorganic NWs on stretchable substrates.[92] In this method, NWs on the as-grown substrate were first transferred to a stretched PDMS substrate by contact printing followed by release of strain afterward.[92] During the strain releasing process, spacing between neighboring NWs was closed up, resulting in parallel alignment of NWs along the direction normal to stretching and an increase of NW surface density.[92] Thereafter, the aligned NW arrays could be transferred again to other rigid or flexible substrates for device fabrication. In this interesting assembly method, the large-strain elasticity of the substrate and the static friction between the NWs and the substrate are the two pivotal factors.[92] In fact, besides transferring bottom-up grown NWs, the similar approach has also been utilized to transfer top-down fabricated Si, GaAs, InAs, and PZT nanomaterials for high-performance flexible electronics and energy harvesting.[98,99,103,104]

Printed Nanowire Arrays for Flexible Electronics. The capability of assembling/printing various NW materials with adjustable atomic composition on flexible substrates in a scalable fashion enables a broad spectrum of applications in flexible electronics. In this review, we focus on inorganic synthetic semiconductor NWs as building blocks for flexible electronics. These materials typically have high carrier mobility which is suitable for fabricating high-frequency/high-performance devices on flexible substrates. For example, catalytically grown Ge/Si core/shell NWs and InAs NWs have been reported with 730 and over 2000 $cm^2/(V \cdot s)$ field-effect carrier mobility.[24,55] Flexible electronics based on these nanomaterials can easily outperform the existing technology based on either a-Si or organic semiconductors. In the following sections, progress on NW-based high-performance devices and integrated circuitry will be reviewed.

NW Parallel Arrays for Ultrahigh Frequency Transistors. With the fast development of personal electronics industry, ultrahigh frequency devices with light weight, low power consumption, and flexibility are in great demand. In this regard, high mobility inorganic semiconductor NWs are naturally ideal candidates. Recently, radio frequency response of InAs NW array transistors on mechanically flexible substrates has been demonstrated by Takahashi *et al.*[69] In this work, InAs NWs were synthesized on Si/SiO_2 substrates by a vapor phase catalytic growth method. Subsequently, NWs are directly transferred from the grown substrate to the polyimide (PI) surface as parallel arrays by the aforementioned contact printing technique. To achieve patterned assembly of NWs, the polyimide surface is first coated with a lithographically patterned resist layer, followed by NW printing and lift-off in a solvent. Nickel source and drain electrodes were then formed,

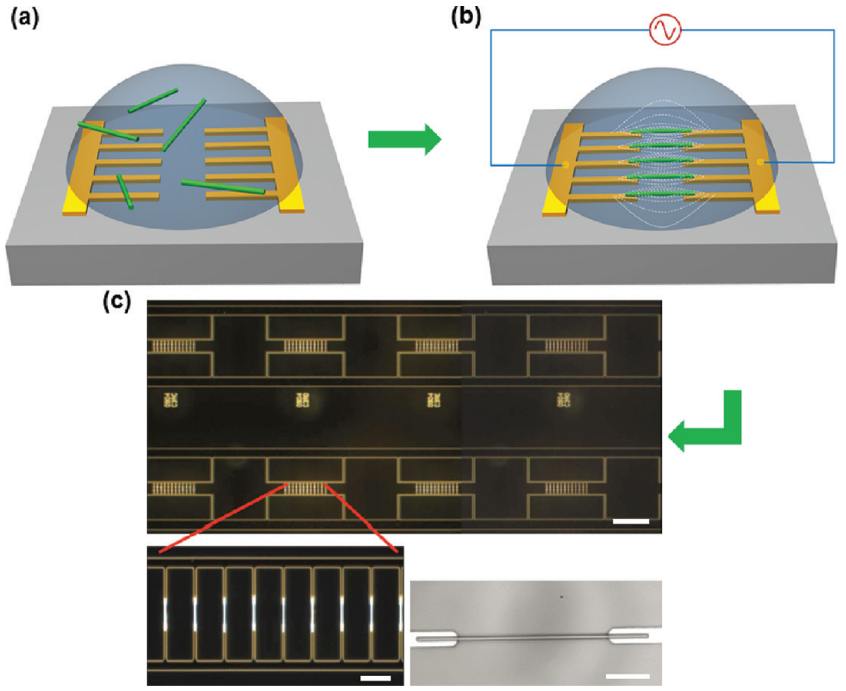

Figure 8. Electric field-assisted NW assembly. (a) Random NWs in the suspension on the electrodes before electric field-assisted assembly. (b) NWs are parallel after electric field-assisted assembly. (c) Optical dark-field images of NWs assembled onto electrodes by electric field-assisted process. Reprinted with permission from ref 79. Copyright 2010 Nature Publishing Group.

followed by atomic layer deposition of Al_2O_3 as the gate dielectric. Finally, Al top-gate (G) electrodes were fabricated. For such devices, the typical channel length (S/D electrode spacing) is $L \sim 1.5\ \mu$m, and the channel width is 100−200 μm.[69] The gate electrode length is $L_G \sim 1.4\ \mu$m. The configuration of the electrical pads matches that of the conventional ground-signal-ground (GSG) microwave probes (150 μm pitch). Figure 9a shows the layered schematic of a NW array RF device. The printed NW density is ~4 NWs/μm, as confirmed by scanning electron microscopy.[69] After the completion of the fabrication process, the polyimide layer is peeled off from the rigid Si/SiO_2 handling wafer, resulting in mechanically flexible device arrays, as shown in Figure 9b.

To directly extract the high-frequency behavior from the devices, the two-port scattering parameters (S parameters) of InAs NW array FETs were measured in the common-source configuration using standard procedures with a vector network analyzer over a frequency range from 40 MHz to 10 GHz.[69] The S parameters were then used to analyze the RF performance of the device (Figure 10a). S_{11}, S_{22}, S_{21}, and S_{12} are, respectively, the reflection coefficient of the input, the reflection coefficient of the output, the forward transmission gain, and the reverse transmission gain. Figure 10b shows various radio frequency metrics of a representative device with channel width of 200 μm, all derived from S parameters. In this result, the unity transit frequency of the current gain (h_{21}) of a transistor is determined to be f_t = 1.08 GHz, and the maximum

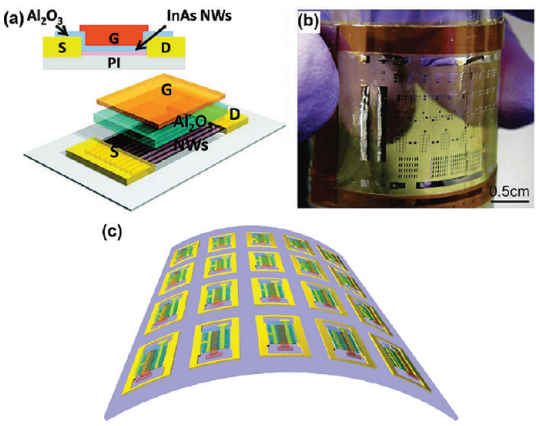

Figure 9. Schematic and optical images of a printed InAs NW array FET fabricated on a flexible polyimide (PI) substrate for GHz operation. (a) Schematic illustration of the NW parallel array FET, illustrating the various layers of the device. The cross-sectional image is shown in the top. (b) Photograph image of the fabricated NW device array on a bendable polyimide substrate. Reprinted from ref 69. Copyright 2010 American Chemical Society.

frequency of oscillation, f_{max}, is found to be 1.8 GHz.[69] The high-frequency response of the device is due to the high saturation velocity of electrons in high-mobility InAs NWs.[69] The results present a scalable platform for integration of ultrahigh frequency devices on flexible substrate, as schematically shown in Figure 1, with potential applications on high-performance digital and analog circuitry.

All-NW Integrated Image Sensor Circuitry. The capability of heterogeneously assembling various types of NWs

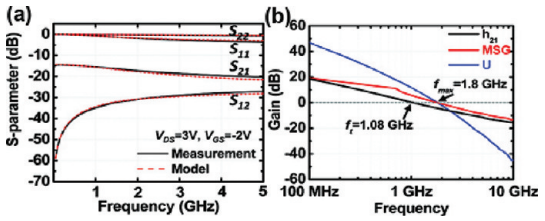

Figure 10. RF characterization of an InAs NW array FET. (a) Measured (black solid line) and modeled (red dashed line) scattering parameters, S_{11}, S_{12}, S_{21}, and S_{22} of an InAs NW array FET with a channel width of ~200 μm after de-embedding for frequencies between 40 MHz and 5 GHz. (b) Current gain (h_{21}), maximum stable gain (MSG), and unilateral power gain (U) extracted from measured S parameters as a function of frequency. The unity current gain frequency, f_t, and unity power gain frequency, f_{max}, are ~1.08 and 1.8 GHz, respectively. Reprinted from ref 69. Copyright 2010 American Chemical Society.

on substrates enables fabrication of NW-based multifunctional integrated circuitry with certain complexity. In this regard, concept-proof all-NW integrated sensor circuitry has been successfully fabricated by Fan *et al.*[70] Figure 13b shows the schematic and circuit diagram of an all-NW photodetector circuit, and Figure 11c shows an optical image (c1) of a fabricated circuit with SEM images (c2−c4) showing details of circuit components. Specifically, each individual circuit includes three device elements: (i) an optical nanosensor (NS) based on either a single or parallel array of CdSe NWs, (ii) a high-resistance FET (T1) based on parallel arrays of 1−5 Ge/Si core/shell NWs, and (iii) a low-resistance buffer FET (T2) with the channel including parallel arrays of ~2000 Ge/Si NWs. These two types of NWs were assembled with a two-step contact printing approach.[70] In the circuitry, T1 was utilized to match the output impedance of the nanosensor in a voltage divider configuration. As a result, the output current of T2 is modulated once the illumination-dependent nanosensor is translated into potential V_{G2}, causing the nanosensor current signal to be amplified by up to 5 orders of magnitude. Figure 11d shows the time-resolved photoresponse measured for several illustration cycles, showing average dark and light currents of ~80 and ~300 μA, respectively.[70]

As contact printing is a scalable technique for NW assembly, large-scale all-NW circuit arrays have been fabricated.[70] Figure 12a shows the optical image of a large array (13 × 20) of the all-NW photodetection circuits, resembling an image sensor.[70] Particularly, each individual circuit of the array functions as a single pixel to respond to incident light. Furthermore, a halogen light source was focused and projected onto the center of the matrix (Figure 12b) to illustrate the image-sensing function of the circuit array, and the photoresponse of each single circuit component was recorded. Eventually, photoresponse of each individual circuit pixel was organized into a gray scale 2D matrix, reflecting the profile of the halogen light source.[70]

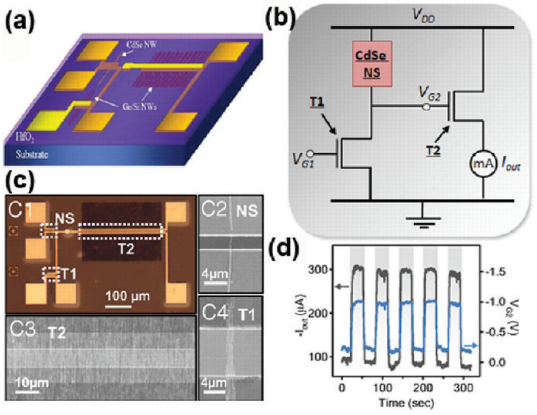

Figure 11. Heterogeneous integration of NWs for an optical sensor circuitry on Si substrates. (a) Schematic of the all-NW optical sensor circuit based on ordered arrays of Ge/Si and CdSe NWs. (b) Diagram of a proof-of-concept NW photosensor circuitry, consisting of a CdSe NW light sensor (NS), an impedance-matching NW transistor (T1), and a buffer transistor (T2). (c1−c4) Optical and SEM images of an all-NW sensor circuitry with the above-mentioned circuit elements. (d) Time-domain response of T2 gate voltage, V_{G2}, and circuit output current, I_{out}, response to light illustration (4.4 mW/cm^2). Reprinted with permission from ref 70. Copyright 2008 The National Academy of Sciences of the USA.

This work has clearly shown that, with the NW printing technique, all-NW integrated circuitry can be realized. As the printing technique has been demonstrated to be highly compatible with a flexible substrate, such integrated circuitry can be realized for flexible electronics in the future.

NW Active-Matrix Circuitry for Artificial Skin. Replacing organic semiconductor or a-Si with inorganic crystalline semiconductor NWs improves performance of flexible electronics. Meanwhile, it enables more functions, particularly those needed to operate in a harsh environment. For example, an electronic skin is expected to be a multifunctional system with integrated sensors responsive to touch, temperature, chemical environment, *etc.* Obviously, sensors themselves and the supporting substrates are required to be flexible in reality. In this regard, researchers have demonstrated an artificial skin based on inorganic semiconductor NWs, and this type of skin can operate at low voltage due to high mobility of NW materials.[19] The structure of the electronic skin device with an integrated NW active-matrix backplane is schematically shown in Figure 13a; it mainly consists of layers of NWs on polyimide, electrode network, and pressure-sensitive rubber as a transducer. Figure 13b shows a photograph of an entirely configured electronic skin with a 19 × 18 pixel matrix consisting of an active area of 7 × 7 cm^2. It shows that the e-skin can readily be bent or rolled to a small radius of curvature, which clearly illustrates the excellent mechanical flexibility of the substrate and its integrated electronic elements. Figure 13c shows an active-matrix circuitry-based sensor array, in which each pixel is dynamically linked to a NW array FET that maintains the pixel state while keeping the other pixels

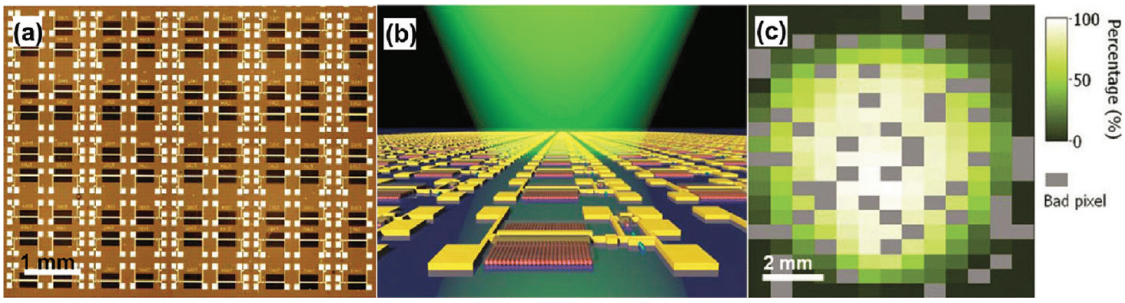

Figure 12. All-NW image sensor on Si substrates. (a) Bright-field optical image of an array of all-NW photosensor circuitry composed of 20 × 13 individual circuits. (b) Perspective picture showing the imaging function of the circuit array. (c) Output response of the circuit array, imaging a circuit light spot. The contrast represents the normalized photocurrent, with the gray pixels representing the defective sites. Reprinted with permission from ref 70. Copyright The National Academy of Sciences of the USA.

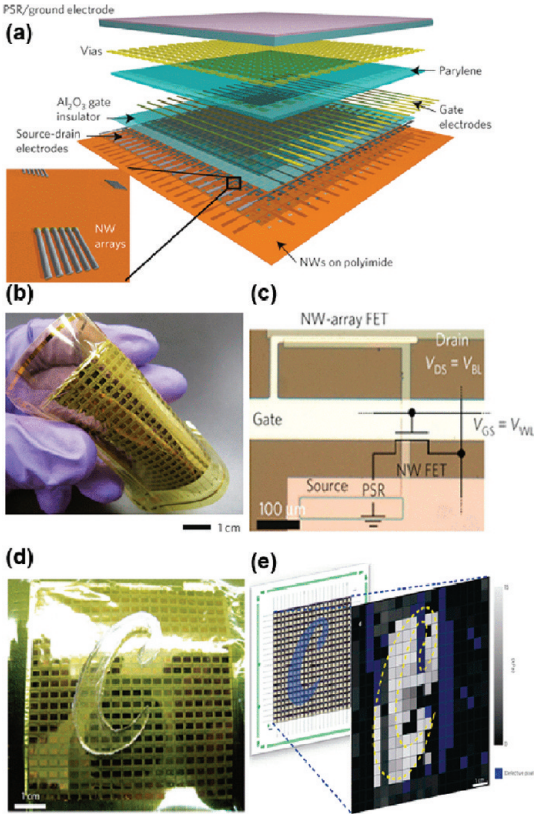

Figure 13. NW-based macroscale flexible devices. (a) Schematic of the passive and active layers of NW e-skin. (b) Optical photographs of a fully fabricated e-skin device (7 × 7 cm^2 with a 19 × 18 pixel array) under bending. (c) Optical microscope image of a single sensor pixel in the array, depicting a Ge/Si NW array FET (channel length ~3 μm, channel width ~250 μm) integrated with a PSR. The circuit structure for the pixel is also shown. (d) Photograph of a fabricated e-skin with a PDMS mold in the shape of "C" placed on the top for applying pressure and subsequent imaging. (e) Corresponding two-dimensional intensity profile obtained from experimental mapping of the pixel signals. The character C, corresponding to the applied pressure profile, can be readily imaged by the e-skin. Reprinted with permission from ref 19. Copyright 2010 Nature Publishing Group.

addressed. This feature shows a prominent advantage over passive-matrix circuitry since the sensor element of passive-matrix circuitry must hold its state with no use of a dynamic switching device. In order to reduce the stochastic device-to-device variation, parallel arrays of NWs were employed as the channel material of the active-matrix FETs.[19] A laminated pressure-sensitive rubber (PSR) is utilized as the sensing component, and the source electrodes of NW array FETs are linked to the ground by PSR. Thus, once the conductance of PSR was altered by applying an external pressure, the NW FET characteristics would be modulated accompanied with the alteration of pixel output signal. Furthermore, to address the word (that is, row) and bit (that is, column) lines of the matrix, respectively, the gate (V_{GS}) and drain (V_{DS}) bias of FETs are employed. As a result, the spatial mapping of the applied pressure can be promptly achieved by addressing and monitoring the conductance of each pixel in the active matrix, as shown in Figure 13d, e. In addition, time-resolved measurements were conducted to explain the response and relaxation time constants of this e-skin device *via* applying an external pressure of ~15 kPa with a frequency of up to 5 Hz while measuring the electrical response of a pixel.[19] In this case, a response and relaxation time of <~0.1 s was measured, and the response of this device did not degrade significantly up to 5 Hz.[19] This test clearly demonstrates the quick and affirmatory response of this e-skin device utilizing high-performance semiconductor NWs.

SUMMARY AND PERSPECTIVE

Crystalline inorganic semiconductor NWs have demonstrated excellent performance for electronics in a broad spectrum of research. Naturally small dimensions make them suitable for nanoscale electronics. Beyond this, their excellent mechanical flexibility, high yield, and low-cost bottom-up synthesis strategies promise a great potential for using these materials for high-performance flexible electronics, aiming at providing an alternative material platform to existing materials, such as organic semiconductors, thin film a-Si, *etc*. Fundamental investigations on the electronic property of semiconductor NWs have been performed extensively. There is no doubt that these materials can offer exciting performance; nevertheless, cost-effective

assembly of NWs remains a bottleneck challenge toward large-scale, practical applications of semiconductor NWs for flexible electronics. In this review, various innovative technologies for large-scale semiconductor NW assembly have been summarized. Some of them, such as NW roll printing, have great potential to be further developed into a roll-to-roll compatible high-throughput NW assembly technology for flexible electronics. Meanwhile, assembled on plastic substrate, some high-performance NWs have demonstrated GHz range operation frequency, which clearly demonstrates the advantage of using crystalline NWs for flexible devices. Last but not least, we have also shown that all-NW integrated circuitry has been implemented and demonstrated designed functionalities. These achievements together have created a solid ground for future exploration of flexible electronics, using crystalline inorganic semiconductor NWs.

Conflict of Interest: The authors declare no competing financial interest.

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